AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings includes changes to Figures 2, 4, and 5.

REMARKS

Drawing Objection; and Claim Rejections under 35 U.S.C. § 112, First Paragraph

The drawings are objected to because it is the Examiner's position that the claimed control unit/means recited in claims 21 and 41-43 is not shown in the drawings. Also, claims 21-24 have been rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement, because it is the Examiner's position that the specification does not disclose the claimed control unit/means.

Figures 2, 4, and 5 are amended to include the control unit/means recited in claims 21 and 41-43. The control unit/means 250 is coupled to the gate terminal of the logic field effect transistor 207 and to the gate terminal of the logic field effect transistor 208.

Support for this amendment can be found in page 15, lines 31-37, of the originally filed specification, where it is mentioned that the control unit can be set up in such a manner that it applies a data signal to the gate terminal of the logic field effect transistor. It is also mentioned in page 24, lines 27-30, of the originally filed specification that either the first n-MOS logic field effect transistor 207 or the second n-MOS logic field effect transistor 208 is conducting (depending on whether the data signal is D="1" or D="0")." Thus, it is clear that the control unit/means 250 should be coupled to the gate terminal of the logic field effect transistor 207 and to the gate terminal of the logic field effect transistor 208.

The paragraphs from page 13 to page 17 of the originally filed specification, which were deleted in the Preliminary Amendment, are added back into the specification by this Amendment. Support for the feature of the control unit/means can be found in these reinstated paragraphs.

Reconsideration and withdrawal of this objection and rejection are respectfully requested.

Claim Objections

Claims 21-24 and 26-41 have been objected to because of informalities.

In response, the phrase "can be" is changed to "is" in claims 21-24 and 26-41.

Claim 34 is amended to be dependent on claim 21. Applicant respectfully submits that amended claim 34 is of proper dependent form. Claims 35-40 which are dependent on amended claim 34 are also in proper dependent form.

Reconsideration and withdrawal of this objection are therefore respectfully requested.

Claim Rejections – 35 U.S.C. § 112, Second Paragraph

Claims 21-24 and 26-40 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Applicant respectfully submits that the term "source/drain" is clear to a skilled person. A field effect transistor (FET) is structurally symmetrical. Therefore, a source terminal and a drain terminal of a FET can be used interchangeably. For example, one terminal of a n-channel metal-oxide-semiconductor FET (MOSFET) is identified as a source terminal if that terminal is connected to a lower voltage supply as compared to the other terminal, and the other terminal which is connected to a higher voltage supply is identified as a drain terminal. For a p-channel MOSFET, one terminal is identified as a drain terminal if that terminal is connected to a lower voltage supply as compared to the other terminal, and the other terminal which is connected to a higher voltage supply is identified as a source terminal.

In view of the above, Applicant respectfully submits that a skilled person is able to identify a source terminal and a drain terminal from the circuit connections as claimed, and also as described in the specification.

The term "a flip flop signal" refers to the flip flop signal Q and the flip flop signal /Q. Support can be found in page 11, lines 10-12, of the originally filed specification. The term "input signal" refers to the signal /S or /R. Support can be found in page 10, line 37, to page 11, line 2, of the originally filed specification. Therefore, it is clear that the flip flop signal is different from the input signal.

For further clarification, claims 21 and 41-43 are amended to delete the term "a flip flop signal." Claims 21 and 41-43 are amended to define "to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated." Support for this amendment can be found in page 10, lines 18-26, of the originally filed specification.

Claim 30 is amended to clarify that the additional transistors of the second signal path include a clock pulse field effect transistor, a logic field effect transistor and a feedback field effect transistor. Claim 30 is also amended to clarify that the additional transistors of the second signal path are interconnected in a same way as the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor of the first signal path, which is defined in claim 21.

The antecedent of "flip flop circuit" is changed from "a" to "the" to clarify that the flip flop circuit recited in claim 34 is the same as the flip flop circuit recited in claim 21. The flip flop circuit recited in claims 35, 36, and 40 are also the same as the flip flop circuit recited in claim 21.

Claim 35 is amended to replace "the input signal and/or the complementary input signal" with "at least one of the input signal and the complementary input signal."

Claims 37 and 38 are amended to replace "further comprising" with "wherein the switching field effect transistors comprise."

Claim 38 is also amended to change the antecedents of "gate terminal" and "complementary bypass field effect transistor" from "the" to "a."

Claim 39 is amended to replace "further comprising" with "wherein the flip flop circuit further comprises."

Claim 40 is amended to define "wherein the flip flop circuit has complementary storage field effect transistors configured to store a complementary storage signal which is complementary to the storage signal." Claim 40 is also amended to be dependent on claim 35.

In view of the above arguments and amendments, Applicant respectfully submits that claims 21-24 and 26-40 comply with 35 U.S.C. § 112. Reconsideration and withdrawal of this rejection are respectfully requested.

Claim Rejections – 35 U.S.C. § 102

Claims 21-23, 26-28, and 30-43 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Kim (U.S. Patent No. 6,486,719).

Kim does not disclose "... to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated," as required by independent claim 21.

In Kim, a latch circuit 41a of Figure 6 has NMOS transistors NA and NB connected in series with each other and in parallel with NMOS pull-down transistor N1. Both the NMOS transistors NA and NB are turned on in combination with the NMOS pull-down transistor N1. See Kim, column 5, lines 51-60.

A latch circuit 41d shown in Figure 9 is a modification of the latch circuit 41a of Figure 6. The latch circuit 41d of Figure 9 has NMOS transistors NA and NB connected in series with each other and in parallel with NMOS pull-down transistor N0. NMOS pull-down transistor N1 is connected in series with the parallel circuit of the serially connected NMOS transistors NA and NB and the NMOS pull-down transistor N0.

Since the latch circuit 41d of Figure 9 is a modification of the latch circuit 41a of Figure 6, the operation of the latch circuit 41d of Figure 9 is similar to the operation of the latch circuit 41a of Figure 6. Therefore, the latch circuit 41d of Figure 9 turns on both the NMOS transistors NA and NB in combination with the NMOS pull-down transistor N0.

Assuming that the NMOS transistor NA corresponds to the clock pulse field effect transistor, the NMOS transistor NB corresponds to the logic field effect transistor, and the NMOS pull-down transistor N1 corresponds to the feedback field effect transistor, Kim does not disclose

that the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated.

In view of the above, Applicant respectfully submits that independent claim 21 is novel over Kim. Being dependent on independent claim 21, claims 22-24 and 26-40 are novel over Kim.

Since independent claims 41-43 include limitations similar to the limitations discussed above with respect to independent claim 21, they are patentable over Kim for at least the same reasons.

In view of the above, Applicant believes the pending application is in condition for allowance.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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